Evaluating the ADF4382A Microwave Wideband Synthesizer with Integrated VCO

FEATURES

- Self-contained evaluation board, including the ADF4382A frequency synthesizer with integrated VCO, loop filter, USB interface, on-board reference oscillator, propagation delay calibration paths, and voltage regulators
- Windows®-based software allows control of synthesizer functions from a PC
- Externally powered by 6 V

EVALUATION KIT CONTENTS

- EV-ADF4382ASD2Z evaluation board

EQUIPMENT NEEDED

- A Windows-based PC with USB port for the evaluation software
- A system demonstration platform, serial only EVAL-SDP-CS1Z controller board (SDP-S)
- Power supply (6 V)
- Spectrum analyzer or phase noise analyzer
- 50 Ω terminators
- Low noise input reference (REF_{IN}) source (optional)

DOCUMENTS NEEDED

- ADF4382A data sheet
- EV-ADF4382ASD2Z user guide

REQUIRED SOFTWARE

- Analysis | Control | Evaluation (ACE) Software, Version 1.26 or newer
- ADF4382A plugin, 1.2023.48200 or newer

GENERAL DESCRIPTION

The EV-ADF4382ASD2Z evaluates the performance of the ADF4382A frequency synthesizer with an integrated voltage-controlled oscillator (VCO) for phase-locked loops (PLLs). A photograph of the evaluation board is shown in Figure 1. The EV-ADF4382ASD2Z contains the ADF4382A frequency synthesizer with an integrated VCO, a USB interface, power supply connectors, on-board reference oscillator, propagation delay calibration paths, and Subminiature Version A (SMA) connectors. The outputs of the EV-ADF4382ASD2Z are AC-coupled with 50 Ω transmission lines, making these outputs suitable to drive 50 Ω impedance instruments.

The EV-ADF4382ASD2Z requires an SDP-S controller board, which is not supplied with the evaluation board kit). The SDP-S allows software programming of the EV-ADF4382ASD2Z with Analog Devices, Inc., ACE software.

Full specifications for the ADF4382A frequency synthesizer are available in the ADF4382A data sheet, which must be consulted in conjunction with this user guide when working with the EV-ADF4382ASD2Z.

EV-ADF4382ASD2Z EVALUATION BOARD PHOTOGRAPH

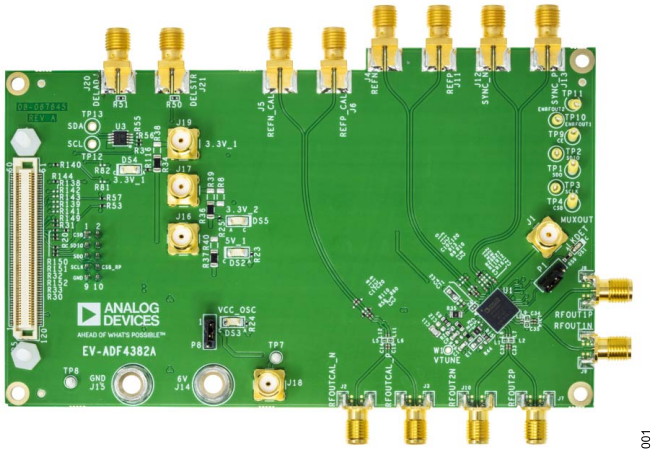

Figure 1. EV-ADF4382ASD2Z Evaluation Board Photograph

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REVISION HISTORY

12/2023—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURE

To install the ADF4382A plugin, take the following steps:

1. Install the latest version of the ACE software platform from the Analysis | Control | Evaluation (ACE) Software web page.
2. Scroll to the **ACE Evaluation Board Plug-ins** selection of the ACE web page
3. In the search bar within the **ACE Evaluation Board Plug-ins** section of the ACE web page, search for ADF4382A and install the chip and board plug-ins that appear.
4. Ensure that the *ADF4382A* plug-ins appear when the EV-ADF4382ASD2Z board is attached through the SDP-S connector to the PC.

EVALUATION BOARD SETUP PROCEDURES

The EV-ADF4382ASD2Z uses a single 6 V power supply with J14 and J15 banana plugs or J18 SMA connector by default. On-board low noise, low dropout (LDO) regulators are used to generate nominal 3.3 V and 5 V supplies.

Details of the power supply circuitry is given in the Power Supplies section.

To power-up the EV-ADF4382ASD2Z, perform the following steps:

1. Set the voltage of the power supply to 6 V and the current limit to 1 A.
2. Connect the power cables to J14 and J15 (two banana cables) or to J18 (single SMA cable).
3. Turn on the power.

To run the **ACE Software**, take the following steps:

1. Select **Start/All Programs/Analog Devices/ACE**.
2. Under the **Select Device and Connection** tab, select the **ADF4382** and the **ADF4382 Board** appears within the **Attached Hardware**.
3. When connecting the EV-ADF4382ASD2Z, allow 5 sec to 10 sec for the label on the **Status** bar to change.
4. Within the **ADF4382 Board** plugin, use the drop-down menu to select the **ADF4382A** before opening the chip plugin.

EVALUATION BOARD HARDWARE

The EV-ADF4382ASD2Z requires the SDP-S platform that uses the EVAL-SDP-CS1Z, which is not supplied with the evaluation kit.

POWER SUPPLIES

The EV-ADF4382ASD2Z is powered by a 6 V power supply connected to the J18 SMA connector, or the J14 banana plug and GND to the J15 banana plug.

The power supply circuitry has three LT3045 high performance, low noise, and low dropout (LDO) regulators and one LT3042 high performance, low noise, and LDO regulator.

One LT3045 is used to generate 5 V to drive the VCO supply pins (V_{5V_VCO}), and the other two LT3045 regulators provide 3.3 V supplies for the 3.3 V Supply Group 1 ($V_{3.3V\_1}$) and 3.3 V Supply Group 2 ($V_{3.3V\_2}$).

The EV-ADF4382ASD2Z provides the flexibility to use external 3.3 V and 5 V supplies with component placement changes detailed in Table 1.

The LT3042 is used to generate 5 V to drive the on-board ultralow, phase noise, sine-wave oscillator.

Table 1. 6 V Component Placement for Power Supplies (DNI Means Do Not Install)

	$V_{3.3V\_1}$		$V_{3.3V\_2}$		V_{5V_VCO}	
6 V Supply	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	0 Ω	DNI	0 Ω	DNI	0 Ω	DNI
Connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector	J14 and J15 banana jack or J18 SMA connector

Table 2. External Supply Component Placement for Power Supplies (DNI Means Do Not Install)

	$V_{3.3V\_1}$		$V_{3.3V\_2}$		V_{5V_VCO}	
External Supply	**R34**	**R38**	**R36**	**R39**	**R37**	**R40**
Component	DNI	0 Ω	DNI	0 Ω	DNI	0 Ω
Connector	J19	J19	J17	J17	J16	J16

EVALUATION BOARD HARDWARE

REFERENCE INPUT

The EV-ADF4382ASD2Z has an on-board, 125 MHz, ultralow phase noise, sine-wave oscillator to drive the ADF4382A reference input. Single-ended oscillator output is connected to the REFP pin, and the REFN pin is AC grounded.

The Y3 reference footprint supports 5 mm × 7.5 mm and 14 mm × 9 mm packages in the 4-pin or 6-pin format. The R87 and R91 resistors can be populated if there is a requirement to set the control voltage of an alternative voltage-controlled crystal oscillator (VCXO).

The default oscillator supply voltage is set to 5 V. If an alternative oscillator requires a different supply voltage, change the R2 resistor on the LT3042 to provide the required supply voltage.

The reference input can also be driven externally via a pair of SMA connectors, REFN (J4) and REFP (J11). When using the external reference, disable the on-board oscillator supply.

Table 3 provides the required board modifications for the external reference clock.

See the ADF4382A data sheet for detailed reference buffer amplitude and frequency considerations.

Table 3. Component Placement for Different Reference Sources

			Differential External Reference	
Component	**Default On-Board Oscillator**	**Single-Ended External Reference**	**CML/LVPECL**	**LVDS**
P8	Short Pin 1 and Pin 2	Short Pin 2 and Pin 3	Short Pin 2 and Pin 3	Short Pin 2 and Pin3
C120	1 µF	Remove	Remove	Remove
C13	Do not install	1 µF	1 µF	1 µF
C110	Do not install	Remove	1 µF	1 µF
R9	0 Ω	0 Ω	Remove	Remove
R10	49.9 Ω	49.9 Ω	Remove	Remove
R13	Do not install	Do not install	100 Ω	100 Ω

EVALUATION BOARD HARDWARE

CLOCK OUTPUTS

The EV-ADF4382ASD2Z has two pairs of SMA connectors for differential clock outputs: RFOUT1P and RFOUT1N, and RFOUT2P and RFOUT2N.

The output power of the clock output channels can be adjusted via the **ACE Software** individually using the **RFOUT1_OPWR** and **RFOUT2_OPWR** numeric selectors (see Figure 5).

The clock output channels can be powered down separately via the **ACE Software** or hardware using the **PD CLKOUT 1** and **PD CLKOUT 2** check boxes (see Figure 5).

If only one port of a differential pair is used, terminate the complementary port with an equal load terminator (in general, a 50 Ω terminator). Refer to the ADF4382A data sheet for more information on output termination examples.

CALIBRATION PATH

The EV-ADF4382ASD2Z has two pairs of SMA connectors for the calibration path input and output: REFN_CAL and REFP_CAL, and RFOUTCAL_N and RFOUTCAL_P. The calibration path is used to measure and calibrate out the board EV-ADF4382ASD2Z effect on the reference to the output delay.

LOOP FILTER

The loop filter schematic is shown in Figure 8. The fifth-order loop filter on the EV-ADF4382ASD2Z is optimized for the ADF4382A low noise amplifier (LNA) reference, a 6 dBm sine-wave reference frequency of 125 MHz, a phase frequency detector (PFD) frequency of 250 MHz, and a charge pump current of 11.1 A. A fourth-order loop filter can be used with faster slew-rate reference signals that allow the use of the delayed match amplifier (DMA) reference of the ADF4382A. Refer to the ADF4382A data sheet for more information on loop filter design.

SERIAL PERIPHERAL INTERFACE (SPI)

Connector P5 interfaces with the SDP-S to evaluate the ADF4382A using the **ACE Software** graphical user interface (GUI). A second connector (P2) is provided for software development. The P2 connector allows a common, open source hardware (OSH) board, such as PMOD, Raspberry Pi, and SDP-K1, to interface directly with the EV-ADF4382ASD2Z.

EVALUATION BOARD HARDWARE

DEFAULT CONFIGURATION

All the necessary components for local oscillator (LO) generation are inserted on the EV-ADF4382ASD2Z. The EV-ADF4382ASD2Z is shipped with a 125 MHz crystal, the ADF4382A synthesizer with an integrated VCO, and a 190 kHz loop filter (with a charge pump current (I_{CP}) = 11.1 mA) at 20 GHz. When the EV-ADF4382ASD2Z is powered up and connected to the **ACE Software**, click **Initialize Device** to provide a 20 GHz output clock on the RFOUT1 channel.

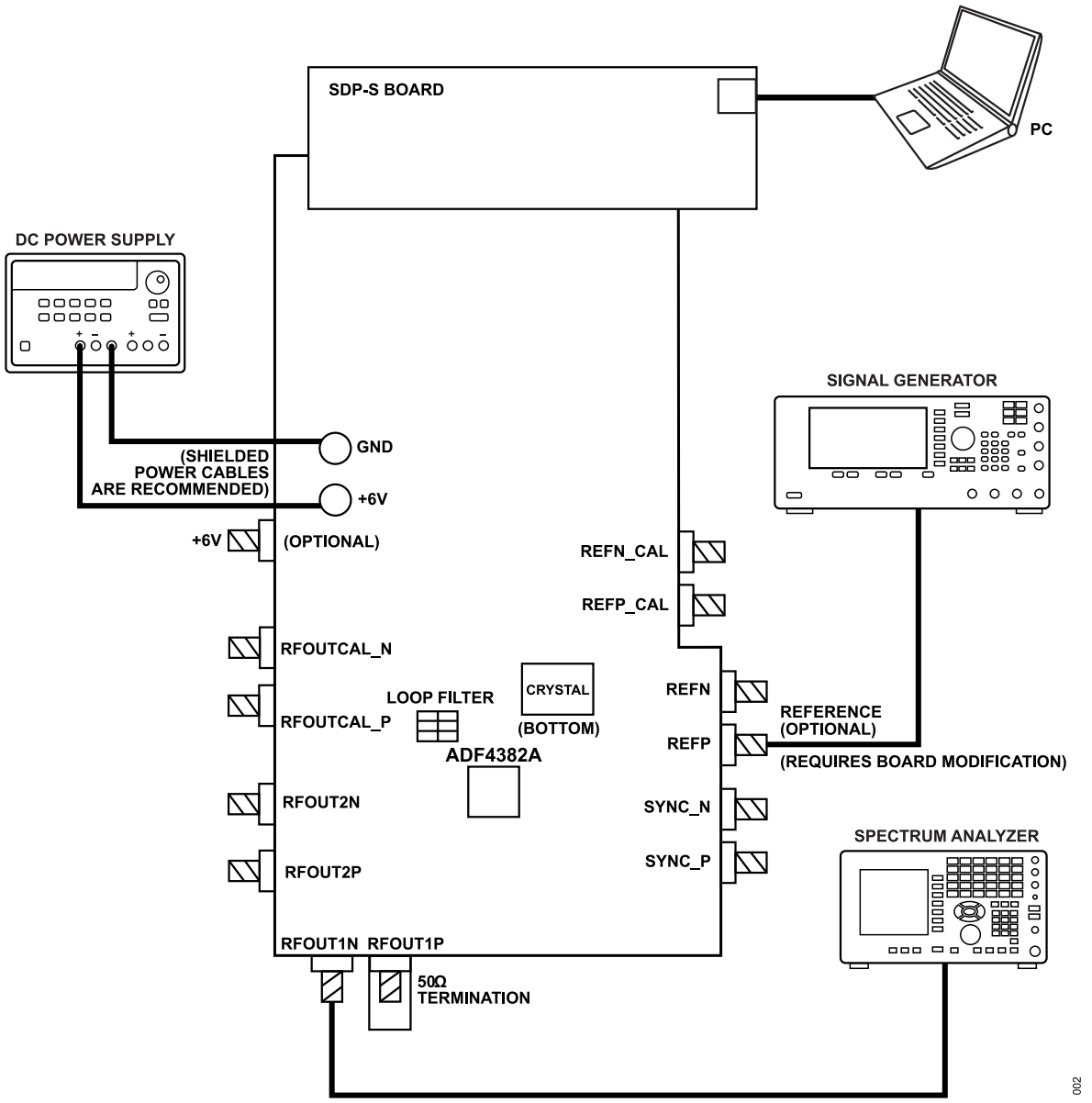


Figure 2. Evaluation Board Setup Diagram

EVALUATION BOARD SOFTWARE

The **ACE Software** is the main platform that is used to control the EV-ADF4382ASD2Z. The ADF4382A plugin includes user interfaces that relate to the ADF4382A and allow evaluation of the device. Use the following steps to open the main control window for ADF4382A:

1. Launch the ACE application. With the SDP-S controller board connected to the EV-ADF4382ASD2Z, the **Attached Hardware** section appears in the GUI, as shown in Figure 3.
2. Double-click the **ADF4382 Board** icon, and the tab shown in Figure 4 appears.
3. Double-click the **ADF4382A** icon that appears on the board GUI to open the main control window shown in Figure 5

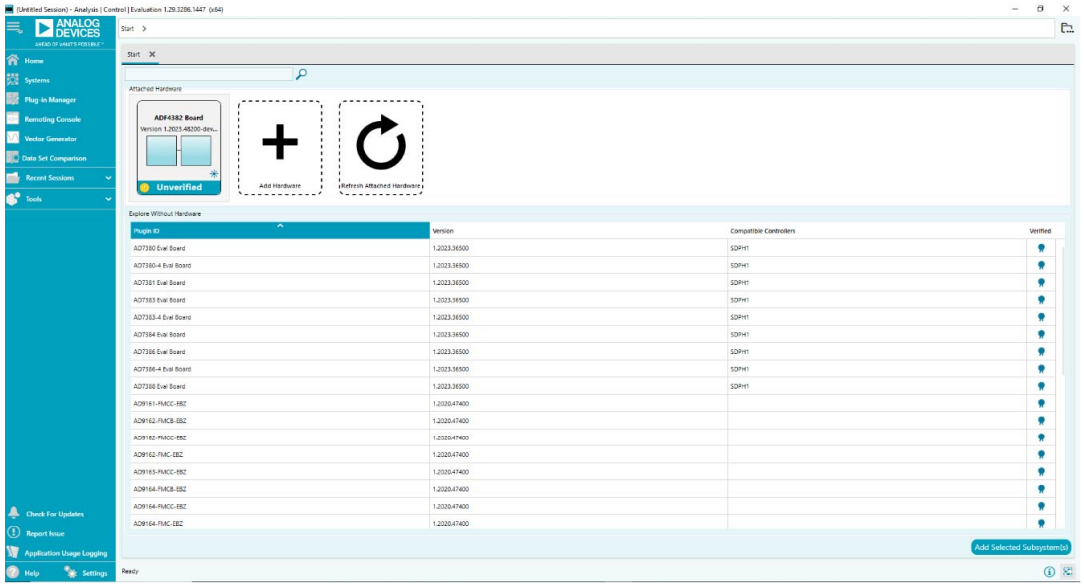


Figure 3. ACE Main Window, Attached Hardware (ADF4382A Evaluation Board)

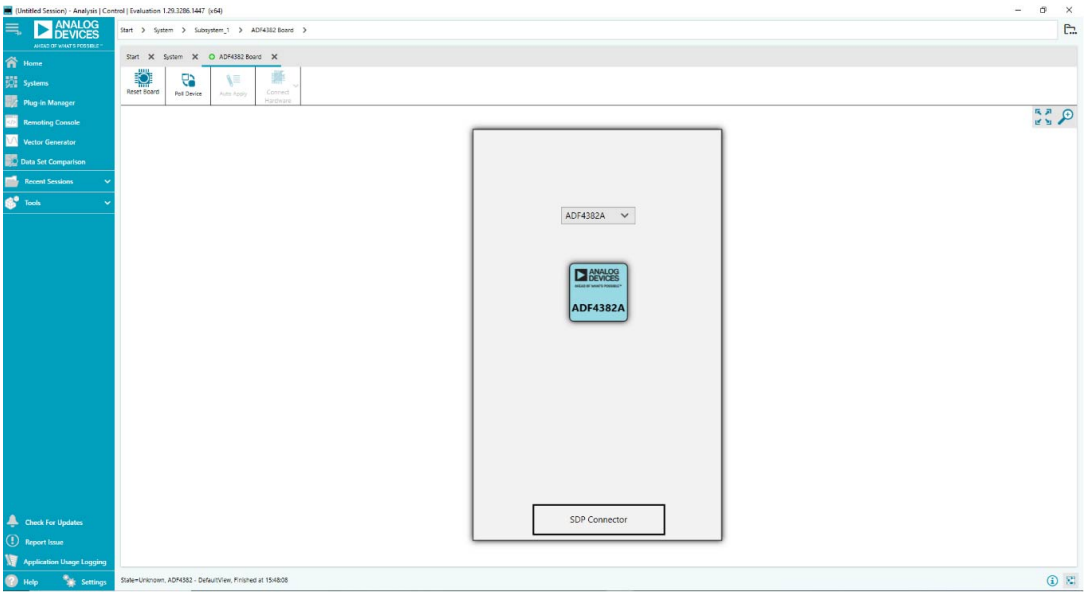


Figure 4. ACE ADF4382A Board Page, Device Selection

EVALUATION BOARD SOFTWARE

MAIN CONTROLS

The main controls are available in the high level register map shown in Figure 5. To modify registers, perform the following steps:

1. Any configuration changes must be done before initializing. The ACE Software plugin opens with the default register settings for a 125 MHz reference frequency, 250 MHz PFD, and 20 GHz output clock frequency.
2. Click **INITIALIZE DEVICE** to write to all registers and to initialize the device (see Figure 5).
3. Modify the front panel settings as required.
4. Click **Apply Changes** to load modified settings to the device. Clicking this button performs the following write sequence:
   a. Programs the changes from the user.
   b. Turns on the clocks necessary for autocalibration.
   c. Triggers an autocalibration by performing a register write to Register 0x010.

If the RFOUT frequency selected is outside of the operational range, an error message appears within the **Errors** section (see Figure 5).

Specific blocks can be powered down by setting the corresponding power-down check box within the **POWER-DOWN** section shown in Figure 5.

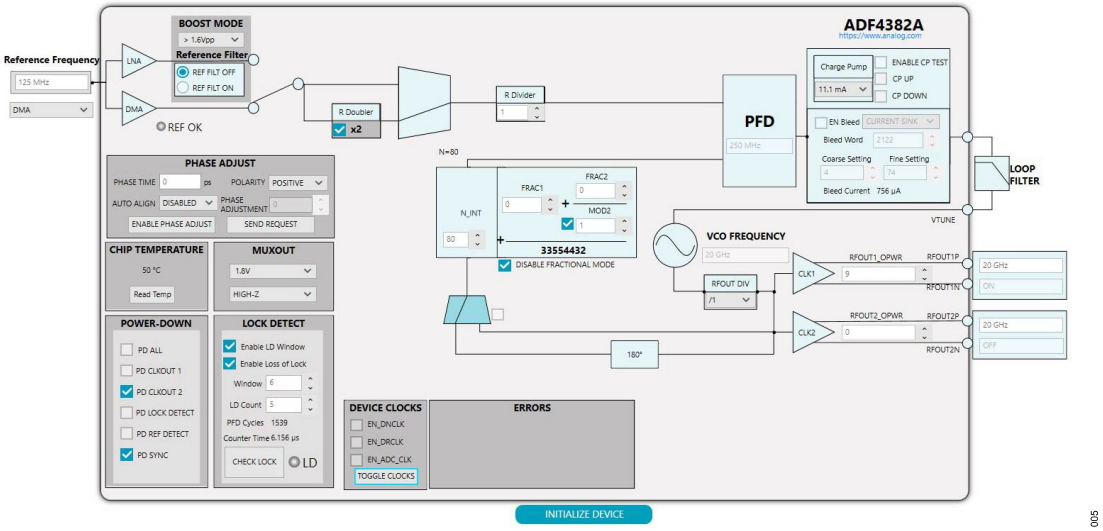


Figure 5. Front Panel

EVALUATION BOARD SOFTWARE

PHASE ADJUSTMENT

The RFOUT phase can be controlled within the **PHASE ADJUST** section in the ACE Software (see Figure 5). To adjust the phase, perform the following steps:

1. Click **Enable Phase Adjust**, to enable the phase adjust feature.
2. Type in the desired phase adjustment in picoseconds in the **Phase Time** box.
3. Select **Positive** or **Negative** polarity for the written phase time using the **POLARITY** drop-down menu.
4. Select **DISABLED** in the **AUTO ALIGN** drop-down menu.
5. Click **SEND REQUEST**.

The actual phase adjustment value is then recorded in the **PHASE ADJUSTMENT** numeric box. Note that the **PHASE TIME** value in picoseconds cannot exceed the period of the **RFOUT** used. For calculations, see the Bleed Current Phase Adjustment section in the ADF4382A data sheet.

FREQUENCY SWEEP

To use the ADF4382A to perform a frequency sweep set the **Start Frequency**, **Stop Frequency**, **Frequency Spacing**, and **Additional Delay (ms)**. If the **Enable VCO Parameter Readback** check box is selected, the corresponding **VCOCore**, **VCOBand**, and **VCOBias** of the configured frequencies is written to the **VCO CAL Bypass** table (see Figure 6).

To perform frequency sweep, take the following steps:

1. Set the **Start Frequency**, **Stop Frequency**, and **Frequency Spacing**.
2. Check off the **Enable VCO Parameter Readback** check box.
3. Click **Start/Stop Sweep**.

Alternatively, click **Run Single Step** instead to perform one frequency step on each button click.

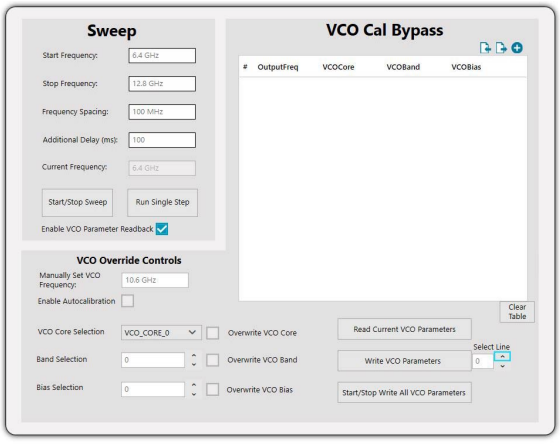


Figure 6. ACE Frequency Sweep

MANUAL VCO CONTROL

The ADF4382A can bypass autocalibration by manually writing predetermined VCO core, band, and bias information. The **VCO Override Controls** section shown in Figure 6 of the ADF4382A plugin can be used to perform an autocalibration bypass.

Take the following steps, to perform the autocalibration bypass:

1. Disable the **Enable Autocalibration** check box by deselecting the check box.
2. Select the **VCO Core Selection** by using the drop-down menu and check off the **Overwrite VCO Core** check box.
3. Set the **Band Selection** value and check off the **Overwrite VCO Band** check box.
4. Set the **Bias Selection** value and check off **Overwrite VCO Bias** check box.
5. Click **Write VCO Parameters**.

Configure the VCO within the **VCO Cal Bypass** table:

1. Click **Read Current VCO Parameters** to read the VCO parameters at the current frequency.
2. Click **Write VCO Parameters** to apply the VCO parameters. Set the **Select Line** box to select the line to apply from the **VCO Cal Bypass** table.
3. Click **Start/Stop Write All VCO Parameters** to apply all the VCO parameters from the **VCO Cal Bypass** table.

EVALUATION AND TEST

To evaluate and test the performance of the ADF4382A, prepare the hardware and software setup as outlined in the Evaluation Board Hardware section and the Evaluation Board Software section.

Run the software and follow the steps given in Evaluation Board Software section to open the main controls shown in Figure 5.

Click INITIALIZE DEVICE to provide a 20 GHz clock at the RFOUT1P and RFOUT1N output. Then, measure the output spectrum and single sideband phase noise on a signal analyzer.

Figure 7 shows a phase noise plot of the SMA RFOUT1P output equal to 20 GHz with a 250 MHz external reference oscillator (250 MHz PFD frequency, buffer selection: DMA buffer, and doubler: disabled).

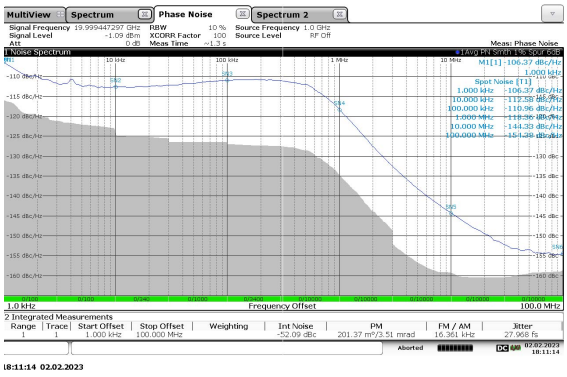


Figure 7. Single Sideband Phase Noise of 20 GHz Output with 250 MHz External Reference

EVALUATION BOARD SCHEMATIC AND ARTWORK

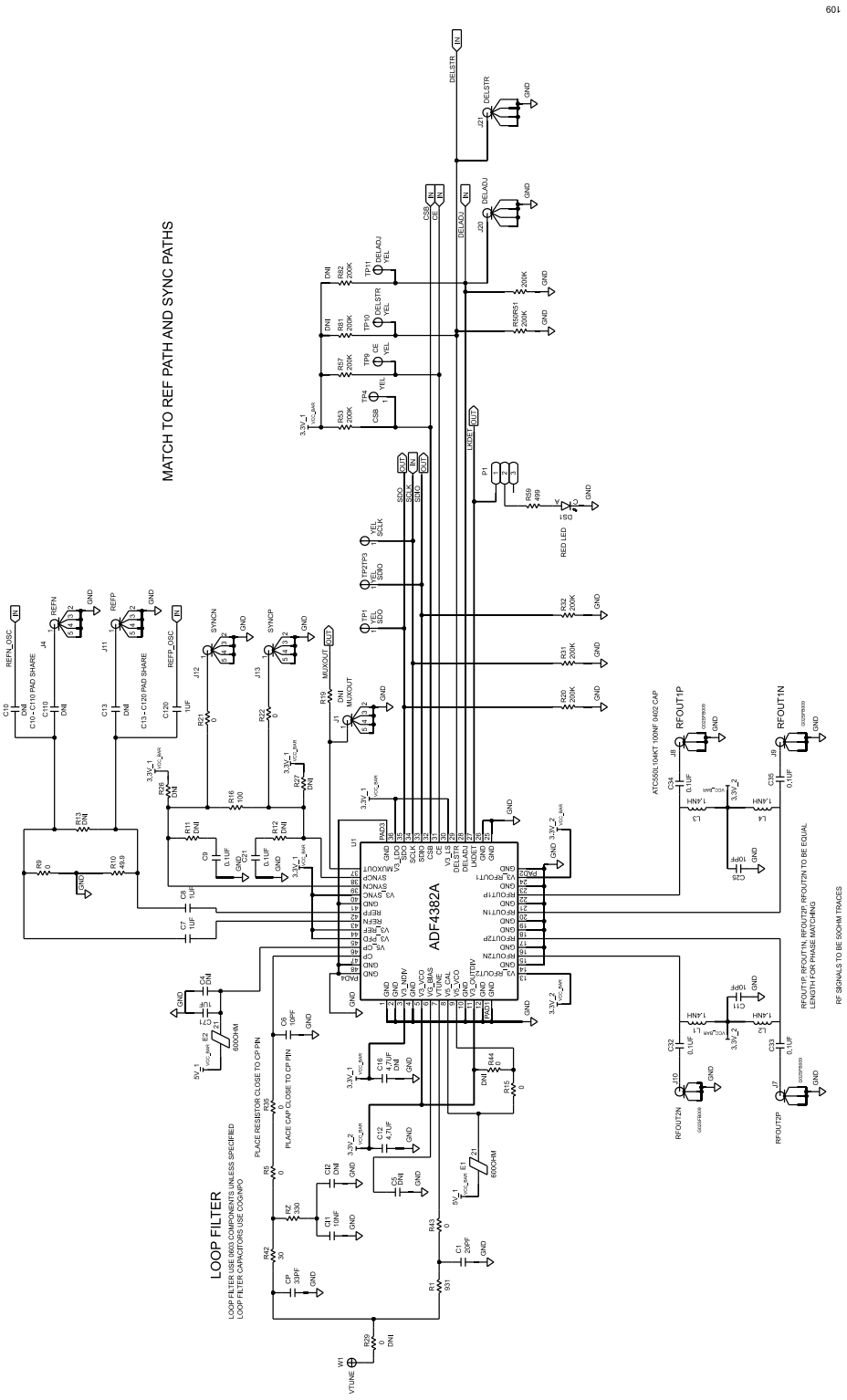
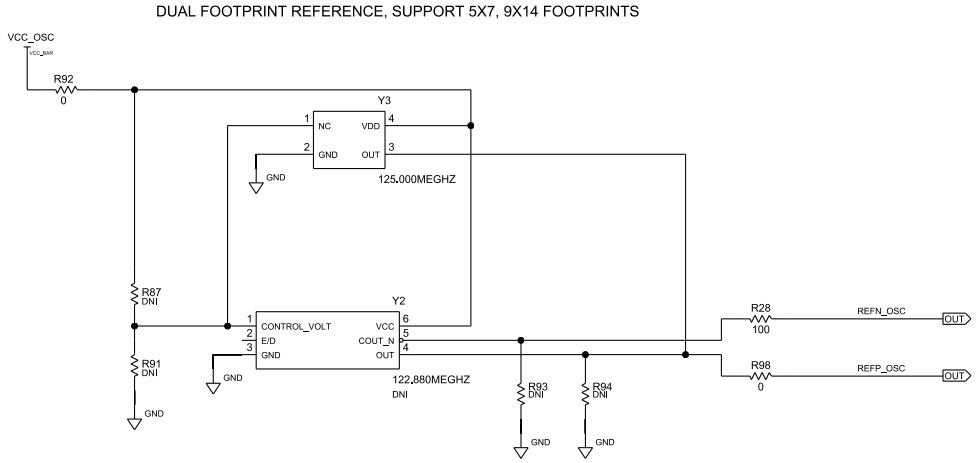


Figure 8. EV-ADF4382ASD2Z Schematic, ADF4382A Connections and Loop Filter

EVALUATION BOARD SCHEMATIC AND ARTWORK



CAL PATH: MATCH TO REF PATH AND CLKOUT PATHS

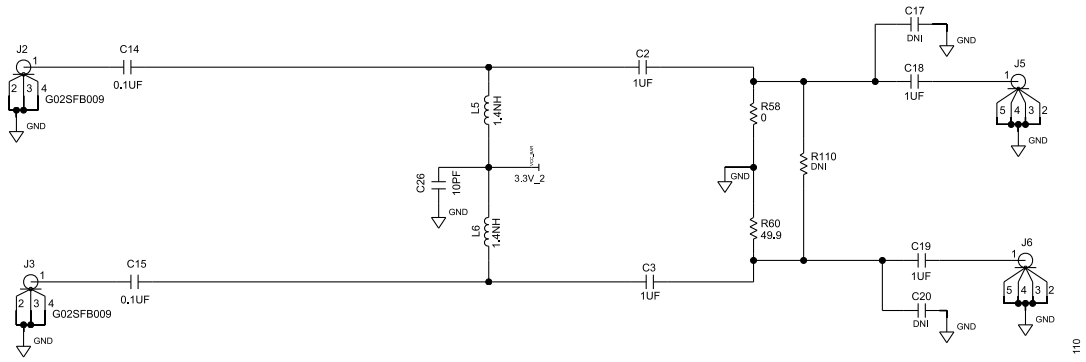


Figure 9. EV-ADF4382ASD2Z Schematic, ADF4382A On-Board Ultra-Low Noise Oscillator, and Calibration Path

EVALUATION BOARD SCHEMATIC AND ARTWORK

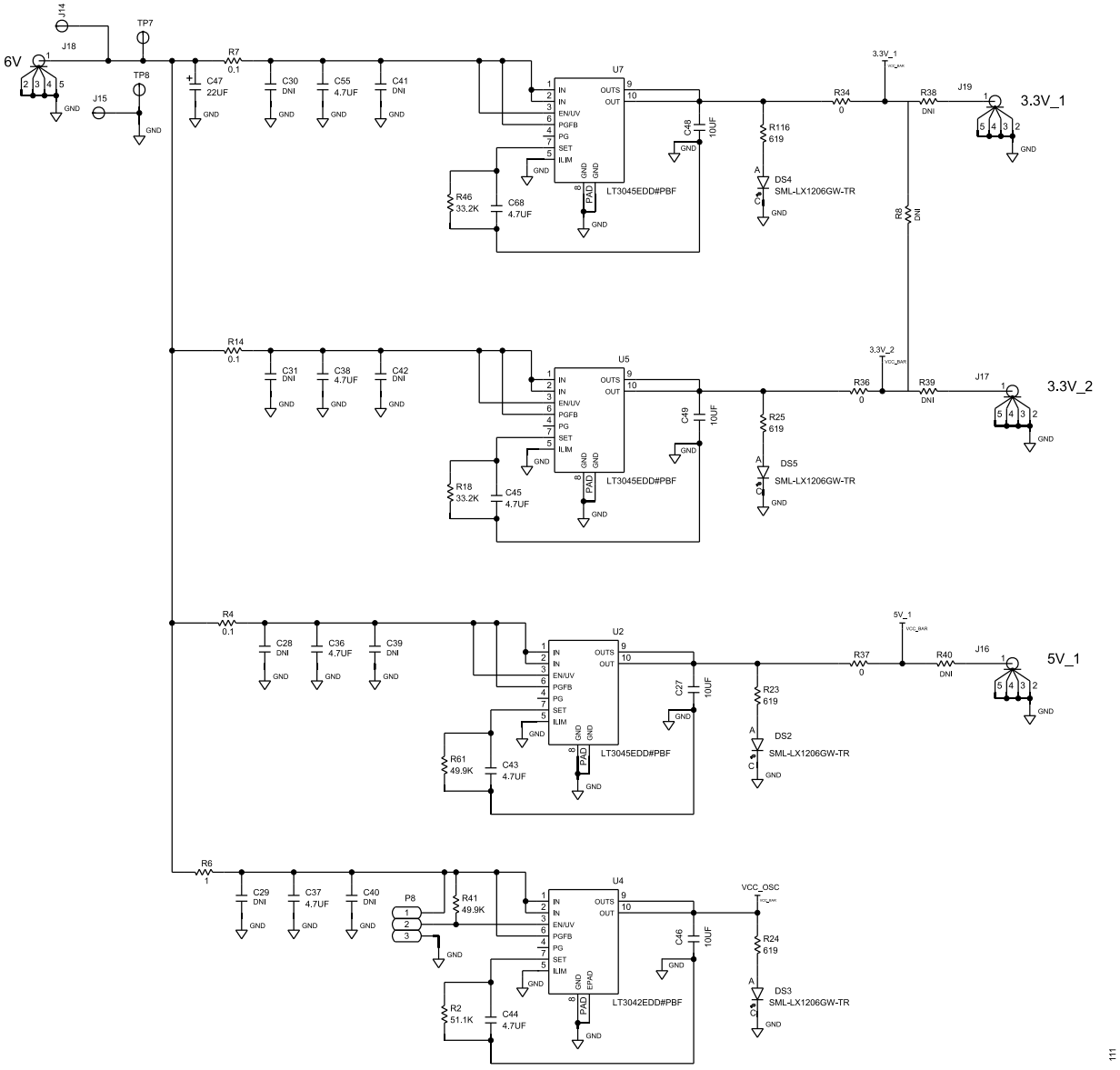


Figure 10. EV-ADF4382ASD2Z Schematic, ADF4382A LDO Regulators

EVALUATION BOARD SCHEMATIC AND ARTWORK

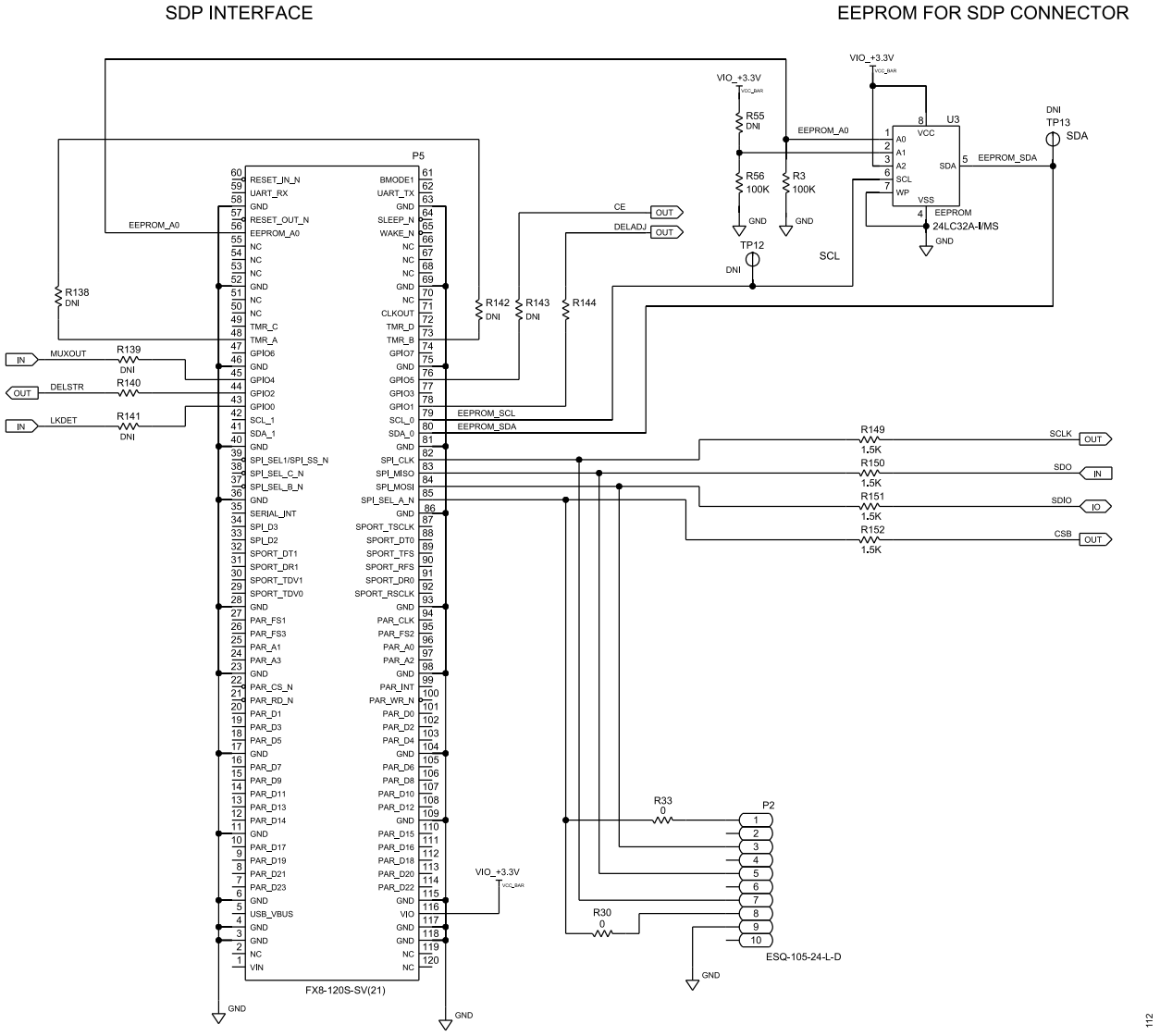


Figure 11. EV-ADF4382ASD2Z Schematic, ADF4382A SDP Interface

EVALUATION BOARD SCHEMATIC AND ARTWORK

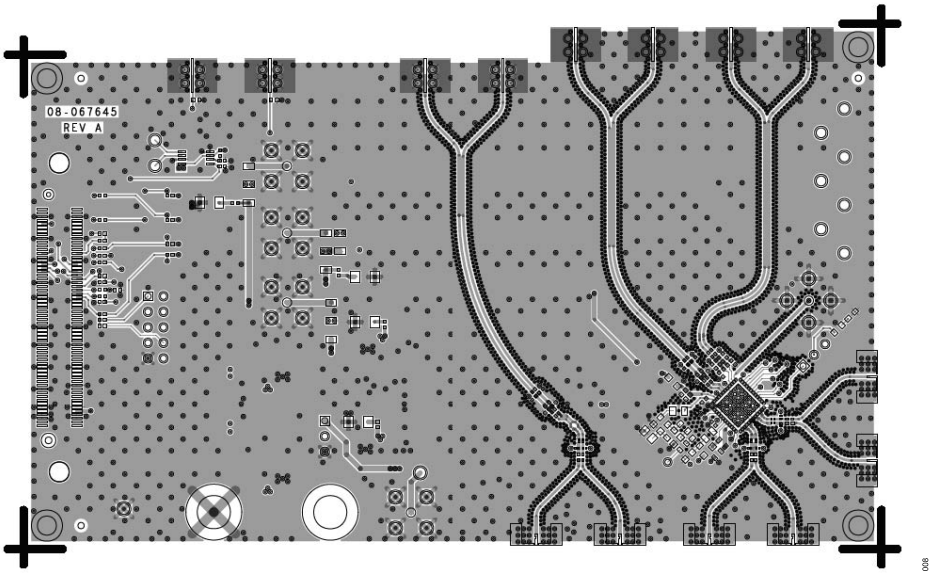


Figure 12. EV-ADF4382ASD2Z Layer 1, Primary

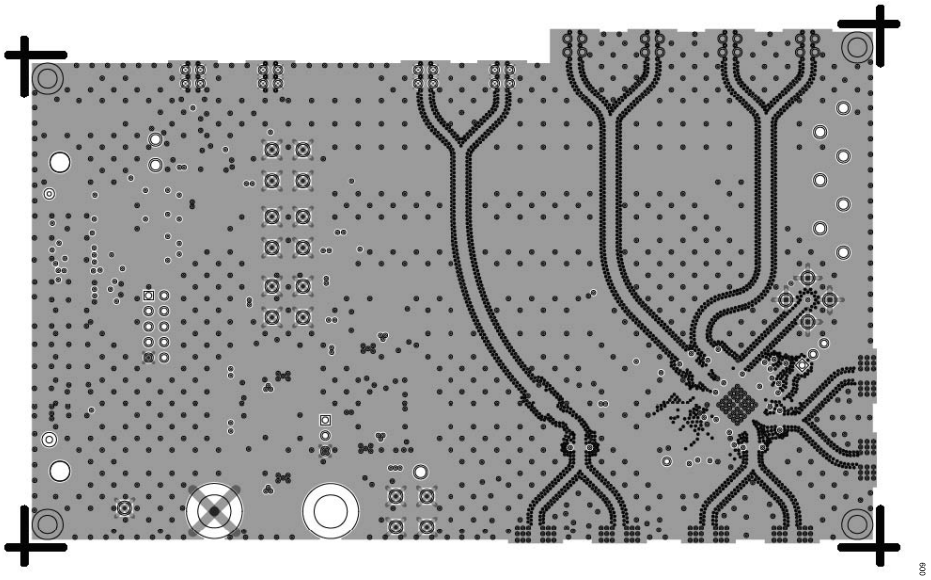


Figure 13. EV-ADF4382ASD2Z Layer 2, Ground

EVALUATION BOARD SCHEMATIC AND ARTWORK

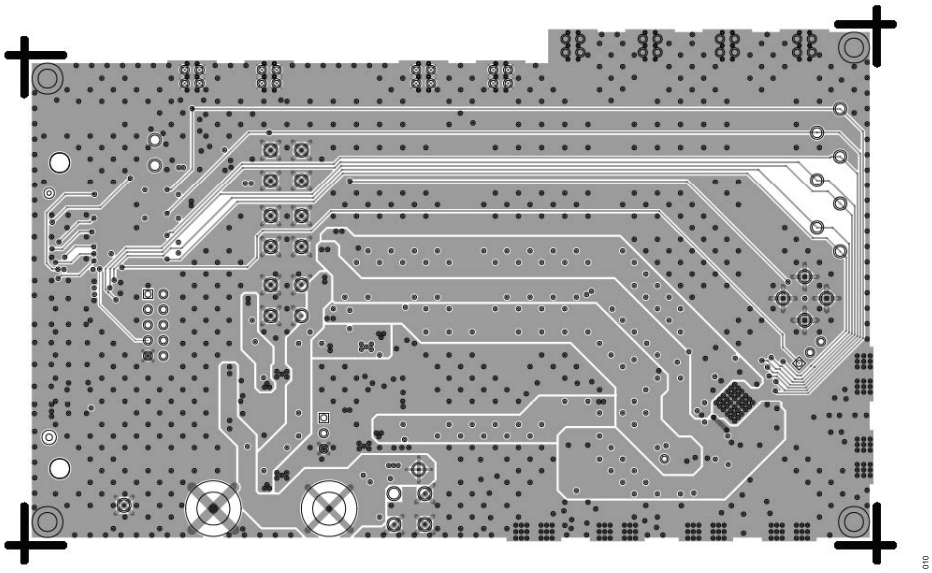


Figure 14. EV-ADF4382ASD2Z Layer 3, Power

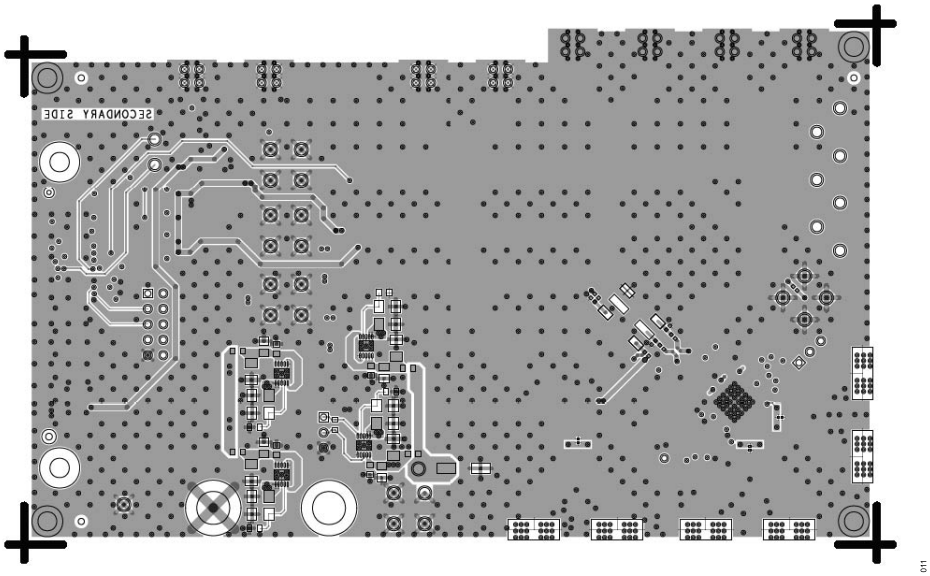


Figure 15. EV-ADF4382ASD2Z Layer 4, Secondary

EVALUATION BOARD SCHEMATIC AND ARTWORK

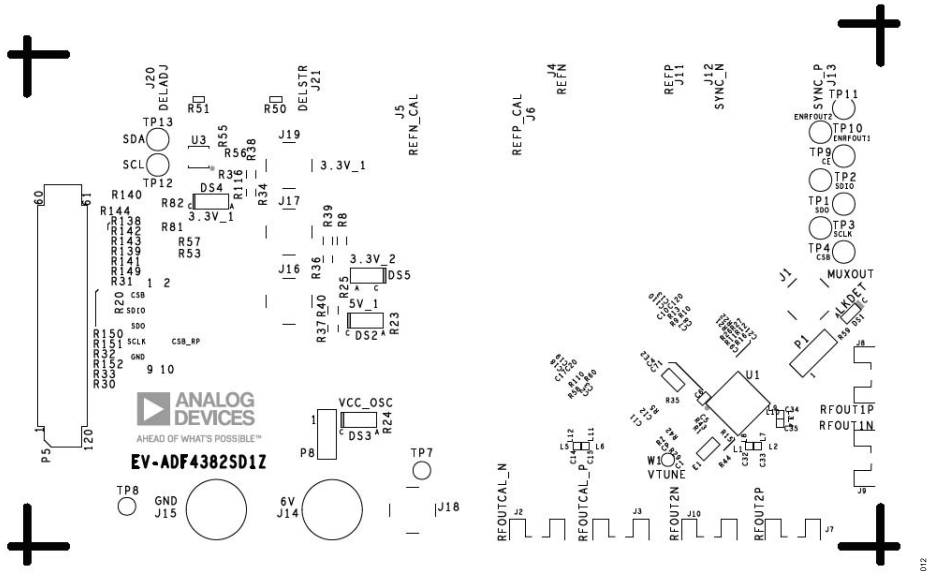


Figure 16. EV-ADF4382ASD2Z Silkscreen, Top Side

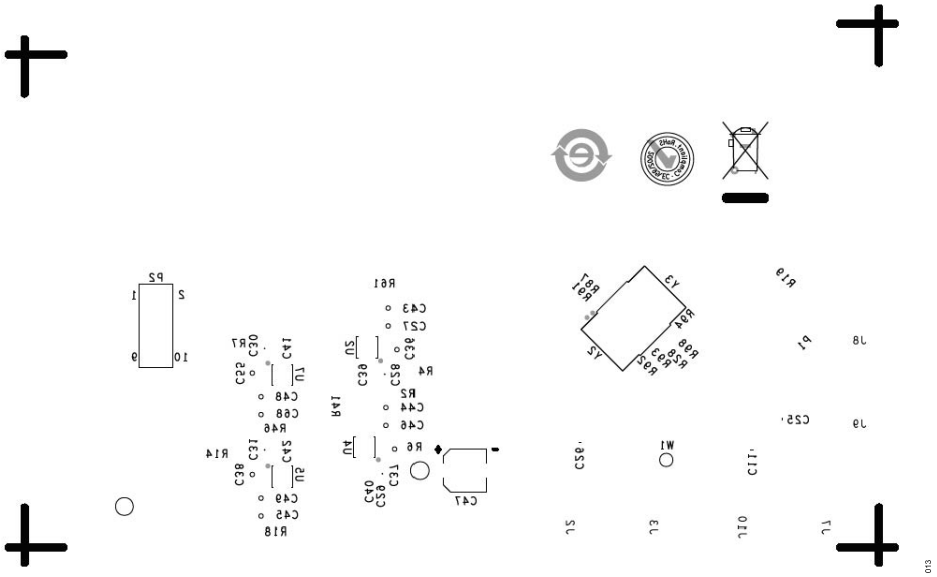


Figure 17. EV-ADF4382ASD2Z Silkscreen, Bottom Side

ORDERING INFORMATION

BILL OF MATERIALS

Table 4. Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
C1	20 pF ceramic capacitor, 50 V, 5%, C0G, 0603, not recommended for new designs (NRND)	Murata	GRM1885C1H200JA01D
C11, C25, C26	10 pF ceramic capacitors, 25 V, 5%, C0G, 0201	Murata	GRM0335C1E100JA01D
C2, C3, C7, C8, C18, C19, C120	1 µF ceramic capacitors, 6.3 V, 10%, X7R, 0402	Murata	GRM155R70J105KA12D
C9, C14, C15, C21, C32, C33, C34, C35	0.1 µF ceramic capacitors, 16 V, 10%, X7R, 0402	Kemet	C0402C104K4RACTU
C27, C46, C48, C49	10 µF ceramic capacitors, 35 V, 10%, X7R, 1206	Taiyo Yuden	GMK316AB7106KL-TR
C36 to C38, C43 to C45, C55, C68	4.7 µF ceramic capacitors, 25 V, 10%, X7R, 1206	Kemet	C1206C475K3RACTU
C47	22 µF capacitor, aluminum, electrolytic, 63 V, 20%, 6.3 mm × 7.7 mm, AEC-Q200	Sun Electronic Industries Corporation	63CE22BSA
C6	200 pF ceramic capacitor, 200 V, 5%, C0G, 0402	Kemet	C0402C221J2GACTU
C71	1 µF ceramic capacitor, 16 V, 10%, 0402, low equivalent series resistance (ESR)	TDK	C1005X6S1C105K050BC
CI1	5100 pF ceramic capacitor, 50 V, 5%, C0G, 0805	Murata	GRM2195C1H512JA01D
CP	150 pF cermanic capacitor, 50 V, 5%, C0G, 0603	Phycomp (Yageo)	2238 867 15151
DS1	Red light emitting diode (LED), surface-mounted device (SMD), 0603	VISHAY	TLMS1100-GS08
DS2 to DS5	Green LED, 565 nM, differential, 1206, SMD	Lumex	SML-LX1206GW-TR
E1, E2	600 Ω inductors, bead chip for power lines	Taiyo Yuden	FBMH1608HL601-T
J1, J16 to J19	Connectors, printed circuit board (PCB), SMA, straight jack, 50 Ω contact center surface mount with thru hole legs	Amphenol RF	132134-15
J2, J3, J7 to J10	Connectors, PCB, 2.92 mm, edge mount jack, DC, 40 GHz	Gigalane	G02SFB009
J4 to J6, J11 to J13, J20, J21	Connectors, PCB, end launch, SMA edge mount square	Emerison Network Power	142-0761-811
J14, J15	Connectors, PCB banana jack	Keystone Electronics	575-4
L1 to L6	1.3 nH inductors, chip, 0.048 Ω DC resistance (DCR), 0.82 A	Coilcraft, Inc.	0201DS-1N3XJEW
L7 to L12	0.5 nH, inductors, RF wirewound chip, 1.25 A, 0.020 Ω DCR	Coilcraft, Inc.	0201DS-0N5XKEU
P1, P8	Connectors, PCB, 3-position, male, unshrouded, single row, straight, 2.54 mm post height, 5.08 mm solder tail	Sametec, Inc.	TSW-103-08-T-S
P2	Connector, PCB, 10-position female header, elevated socket, dual row, straight, 0.64 mm square post, 9.65 mm solder tail, 2.54 mm pitch	Sametec, Inc.	ESQ-105-24-L-D
P5	Connector, PCB, vertical type, receptacle for SDP-S breakout board for electromagnetic interference test use	HRS	FX8-120S-SV(21)

ORDERING INFORMATION

Table 4. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
R1	931 Ω resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF9310V
R10, R60	49.9 Ω resistors, SMD, 1% 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
R23 to R25, R116	619 Ω resistors, SMD, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF6190X
R4, R7, R14	0.1 Ω resistors, SMD, 1%, 1/3 W, 0603, AEC-Q200	Panasonic	ERJ-3BWFR100V
R140, R144, R149 to R152	1.5 kΩ resistors, SMD, 1%, 1/16 W, 0402, AEC-Q200	Stackpole Electronics, Inc.	RMCF0402FT1K50
R5, R15	0 Ω resistors, SMD, jumper, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEY0R00V
R16, R28	100 Ω resistors, SMD, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1000X
R18, R46	33.2 kΩ resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF3322V
R2	51.1 kΩ resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF5112V
R20, R31, R32, R50, R51, R53, R57	200 kΩ resistors, SMD, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF2003X
R9, R21, R22, R30, R33, R58, R92, R98	0 Ω resistors, SMD, jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
R3, R56	100 kΩ resistors, SMD, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1003X
R34, R36, R37	0 Ω resistors, SMD, 5%, ¼ W, 1206, AEC-Q200	VISHAY	CRCW12060000Z0EA
R35, R43	0 Ω resistors, SMD, 1/8 W, 0805, AEC-Q200	Panasonic	ERJ-6GEY0R00V
R41, R61	49.9 kΩ resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4992V
R42	150 Ω resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF1500V
R59	499 Ω resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF4990V
R6	1 Ω resistor, SMD, 5%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3GEYJ1R0V
RZ	200 Ω resistor, SMD, 1%, 1/10 W, 0603, AEC-Q200	Panasonic	ERJ-3EKF2000V
TP1 to TP4, TP9 to TP11	Connector, PCB, yellow test points	Components Corporation	TP-104-01-04
TP7, TP8	Connectors, PCB, solder terminal turrets for clip leads	MILL-MAX	2308-2-00-80-00-00-07-0
U1	Microwave wideband synthesizer with integrated VCO	Analog Devices, Inc.	ADF4382A
U2, U5, U7	20 V, 500 mA, ultralow noise, ultrahigh, power supply rejection ratio (PSRR) linear regulator	Analog Devices	LT3045EDD#PBF
U3	32 KBIT serial, electrically erasable programmable read-only memory (EEPROM)	Microchip Technology	24LC32A-I/MS
U4	20 V, 200 mA, ultralow noise, ultrahigh PSRR RF linear regulator	Analog Devices	LT3042EDD#PBF

ORDERING INFORMATION

Table 4. Bill of Materials (Continued)

Reference Designator	Description	Manufacturer	Part Number
Y3	125.000 MHz, crystal ultralow, noise sine-wave clock oscillator	Crystek Corporation	CCSS-945X-25-125.000

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Analog Devices Inc.:

EV-ADF4382ASD2Z